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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,121	MATHIEU ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-27* is/are pending in the application.

4a) Of the above claim(s) *18-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-17,24-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/30/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I (Claims 12-17 and 24-27) in the reply filed on 02/22/2005 is acknowledged. The traversal is on the ground(s) that search and examination of the entire application can be made without serious burden. This is not found persuasive because Group II is properly classified in 326/16 comprising 434 patents and published applications not previously searched in the current examination of Group I.

The requirement is still deemed proper and is therefore made FINAL.

Specification

2. The disclosure is objected to because of the following informalities: the Applicant uses the term "instruction to be tested" to refer to an instruction that is to be used for testing a processor whereas the term "instruction to be tested" implies that the instruction is being tested. The Examiner would like to point out that nowhere in the Application does the Applicant teach verification of instructions.

Appropriate correction is required.

Claim Objections

3. Claims 12-17 and 24-27 are objected to because of the following informalities: Claims 12-17 and 24-27 use the term "instruction to be tested" to refer to an instruction

that is to be used for testing a processor whereas the term "instruction to be tested" implies that the instruction is being tested. Examiner would like to point out that the preamble of claims 12 and 24 recite, "a selftest procedure to validate behavior of a processor model to be tested" not a procedure to validate instructions. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12-17 and 24-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites, "the at least one instruction to be tested" in lines 10, 12, 15, 19-20 and 21-22, which by its very nature is indefinite since "at least one instruction to be tested" in lines 5-6 can be 1 or 1000 instructions and cannot provide antecedent basis since it is not clear which of the instructions to be tested, "the at least one instruction to be tested" refers to.

Claims 13 and 24 recite, "the at least one instruction to be tested comprises at least two instructions from the set of instructions of the processor model". See prior comments.

Claim 24 recites, "the at least one instruction to be tested" in line 7, which by its very nature is indefinite since "at least one instruction to be tested" in lines 11-12, 14-15, 17-18, 21-22 and 24-25 can be 1 or 1000 instructions and cannot provide antecedent basis

since it is not clear which of the instructions to be tested, "the at least one instruction to be tested" refers to.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 12-15 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Werner; Jeffrey A. et al. (US 5377122 A, hereafter referred to as Werner).

35 U.S.C. 103(a) rejection of claims 12 and 24.

Werner teaches a method verification of a generated circuit model performed automatically by comparing the operation of the circuit model with that of a corresponding mathematical behavior model (see Abstract in Werner), the method

comprising the steps of: receiving specifications from a user including at least one pattern to be tested from among a set of patterns of the circuit model (col. 2, lines 60-62 in Werner teach that circuit models may be verified using the user's chosen input signal, i.e., using the user's chosen pattern to be tested); reading, in a table, characteristic data of the circuit model to be tested (col. 6, lines 3-9 in Werner teaches that global look-up table is used to create circuit modes having characteristics of the actual corresponding circuit implemented in the particular technology selected), the data comprising a functional definition of the at least one pattern to be tested (col. 6, lines 31-35 in Werner teaches that a test pattern fire is created comprising test input signals; Note: a test input signal is a pattern to be tested) and a functional definition of elements of the circuit model (Col. 6, lines 20-30 teach that a behavioral model is created; col. 2, lines 16-22 in Werner teach that a behavioral model is simple a mathematical model representing the actual functional behavior of the circuit); executing the at least one pattern to be tested using the circuit model (Step 8 in Figure 5 of Werner teaches executing all test pattern vectors on the circuit logic model); computing an expected result following execution of the at least one pattern to be tested from the specifications from the user and the characteristic data of the circuit model (Step 9 in Figure 5 of Werner teaches executing all test pattern vectors of the Behavioral model; Note: since the behavioral model is a mathematical model representing the **actual** functional behavior of the circuit, the output of the simulation using the Behavioral model are expected values used to determine whether the circuit logic model is functioning as expected); and causing the circuit model to carry out a self-test procedure to validate the at least one pattern to be tested

(Col. 2, lines 9-12 in Werner teaches that testing is performed automatically using a single logic compiler hence the electronic apparatus in Werner is capable of self-test), the self-test procedure comprising initializing the elements of the circuit model (Step 3 in Figure 5 of Werner), executing the at least one pattern to be tested and obtaining a result (Step 8 in Figure 5 of Werner), comparing the obtained result and the expected result (Step 10 in Figure 5 of Werner), and returning a result word that is equal to a first value if the behavior of the circuit model is right and a second value if the behavior of the circuit model is not right (Col. 7, lines 9-12 in Werner teach that, if the comparison of the output files indicates an output of the circuit logic model is different than the corresponding output of the behavior model, these lines of the output files are written into a difference table; Note: a null entry or no entry into the difference table clearly indicates correct operation of the circuit).

However Werner does not explicitly teach that the circuit model is a model intended for use as processor model using instructions as test patterns.

The Examiner asserts that a processor model is a circuit model since processors are circuits comprised of circuit logic and instructions are test pattern data for testing the functional limitations of processor logic, hence the electronic apparatus in Werner applies to and was intended for use processor model testing and furthermore does not require any substantial structural changes to the electronic apparatus taught in Werner. See Ex parte Masham, 2 USPQ2d 1647 (1987).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to with the teachings of Werner by including an embodiment of the

electronic apparatus in Werner for generating processor models. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that an embodiment of the electronic apparatus in Werner for generating processor models would have provided the opportunity to verify processor models and since use of the electronic apparatus in Werner requires no structural change since a processor model is a circuit logic model. See Ex parte Masham, 2 USPQ2d 1647 (1987).

35 U.S.C. 103(a) rejection of claims 13 and 25.

Steps 8 and 9 in Figure 5 of Werner.

35 U.S.C. 103(a) rejection of claims 14 and 26.

Werner teaches determining if the result word is equal to the first value or the second value (Col. 7, lines 9-12 in Werner teach that, if the comparison of the output files indicates an output of the circuit logic model is different than the corresponding output of the behavior model, these lines of the output files are written into a difference table; Note: a null entry or no entry into the difference table clearly indicates correct operation of the circuit); carrying out an additional self-test procedure if the result word is equal to the first value and if another self-test procedure has to be executed (See "Are Outputs the same?" and "Fetch Next Line" blocks in Figure 5 of Werner); ending the method if the result word is equal to the first value and if another self-test procedure does not have to be executed (See "Are Outputs the same?", "Write the Two Lines Into a

Difference Table" and "Is This the Last NET File?" blocks in Figure 5 of Werner); and storing information for the self-test procedure if the result word is equal to the second value and ending the method, the information comprising an address at which an error has been detected (See "Write the Two Lines Into a Difference Table" block in Figure 5 of Werner; Note: the actual lines are stored in the difference table, which gives a clear indication of address locations).

35 U.S.C. 103(a) rejection of claims 15 and 27.

Werner teaches receiving specifications from the user for at least two self-test procedures; reading, in a table, characteristic data of the processor model necessary for the execution of the at least two self-test procedures (col. 2, lines 60-62 in Werner teach that circuit models may be verified using the user's chosen input signal, i.e., using the user's chosen pattern to be tested; col. 6, lines 3-9 in Werner teaches that global look-up table is used to create circuit modes having characteristics of the actual corresponding circuit implemented in the particular technology selected); and successively computing an expected result for each of the at least two self-test procedures (See "Is This the Last NET File?" block in Figure 5 of Werner).

5. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Werner; Jeffrey A. et al. (US 5377122 A, hereafter referred to as Werner) in view of Akin; Benjamin P. et al. (US 6182245 B1, hereafter referred to as Akin).

35 U.S.C. 103(a) rejection of claims 16 and 17.

Werner substantially teaches the claimed invention described in claims 12-14 (as rejected above).

However Werner does not explicitly teach the specific use of a statistical study to estimate test coverage.

Akin, in an analogous art, teaches use of a statistical study to estimate test coverage (col. 5, lines 4-9 in Akin).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Werner with the teachings of Akin by including an additional step of use of a statistical study to estimate test coverage. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a statistical study to estimate test coverage would have provided test reports for analyzing test coverage.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Primary Examiner
Art Unit 2133